TITLE OF THE INVENTION
FILTER CALIBRATION AND APPLICATIONS THEREOF

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to calibration of circuits of the integrated circuit.

DESCRIPTION OF RELATED ART

Integrated circuits are known to be used in a wide variety of electronic equipment including radios, cellular telephones, wireless modems, home appliances, etc. One common technology for producing integrated circuits is Complimentary Metal Oxide Semiconductor, which is more commonly known as CMOS. CMOS technology has become the fabrication technology of choice for a majority of commercial grade integrated circuits due to its flexibility of design, level of integration, and cost.

While CMOS technology offers many advantages, there are some limitations. For instance, component tolerances of on-chip resistors, capacitors, and/or transistors are at best +/- 5%, but more typically +/- 20%. For many circuits, the component tolerance is not a critical issue, however, for precision circuit the component tolerance is a critical issue. For example, a resistor-capacitor (e.g., RC) low pass filter passes signals having frequencies below a corner frequency of the low pass filter and attenuates signals having frequencies above the corner frequency. As is known, the corner frequency is established based on the resistance value and capacitance value. With component tolerances of +/- 20%, the corner frequency of a single pole RC low pass filter (i.e., a low pass filter that includes a single resistor and a single capacitor) may vary from 0.64 of the desired corner frequency when the R and C are each at the minimum component value to 1.44 of the desired corner frequency when the R and C are each at the maximum component value. This wide variation is unacceptable.

To reduce the adverse affects of the component tolerance variation, many CMOS integrated circuit (IC) designs include an RC calibration circuit and selectable resistor circuits and capacitor circuits for use in precision circuits. In general, the RC calibration circuit includes a test resistor and a test capacitor. The test resistor and test capacitor are tested, typically by applying a voltage, a pulse, and/or a ramp, to determine their actual values. The actual values are compared to the designed values to determine a difference. The difference is used to tune the selectable resistor circuits and capacitor circuits. For example, if the test resistor was designed to be a 1 Kilo-Ohm resistor and it is measured to be 900 Ohms, the actual value is 90 % of the desired value. To achieve the desired value, the actual value must be increased by 1.11 (e.g., 1/0.9). Thus, the selectable resistor and capacitor circuits are adjusted by a value of 1.11.

While the RC calibration circuits allow for precision circuits to be implemented on ICs using CMOS technology, they are based on the assumption that the components of the IC have the same component offset as the test components. In many applications, this assumption is of no consequence. For highly precise circuits, such as low pass filters used in radio receivers to block local oscillation leakage, the RC calibration circuit are not sufficiently accurate.

Therefore, a need exists for a method and apparatus to calibrate highly precise IC circuits including filters.

BRIEF SUMMARY OF THE INVENTION

The filter calibration techniques of the present invention substantially meet these needs and others. In one embodiment, a method for calibrating a filter begins with the filter filtering a first signal having a first frequency to produce a first filtered signal, wherein the first frequency is in a known pass region of the filter. The processing continues by measuring signal strength of the first filtered signal to produce a first measured signal strength. The processing continues with the filter filtering a second signal having a second frequency to produce a second filtered signal, wherein the second

frequency is at a desired corner frequency of the filter. The processing continues by measuring signal strength of the second filtered signal to produce a second measured signal strength. The processing continues by comparing the first measured signal strength with the second measured signal strength to determine whether the filter has attenuated the second signal by a desired attenuation value with respect to the first signal. The processing continues by adjusting filter response of the filter to produce an adjusted filter response when the filter has not attenuated the second signal by the desired attenuation value with respect to the first signal. With such a method and apparatus implementing such a method, components of a highly precise circuit on an integrated circuit may be accurately tuned to provide the desired circuit performance.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a schematic block diagram of a wireless communication system in accordance with the present invention;

Figure 2 is a schematic block diagram of a wireless communication device in accordance with the present invention;

Figure 3 is a schematic block diagram of a filtering module with calibration in accordance with the present invention;

Figure 4A is a graph of a filter response of a low pass filter;

Figure 4B is a graph of testing a low pass filter in accordance with the present invention;

Figure 5A is a graph of a filter response of a high pass filter;

Figure 5B is a graph of testing a high pass filter in accordance with the present invention;

Figure 6A is a graph of a filter response of a bandpass filter;

Figure 6B is a graph of testing a bandpass filter in accordance with the present invention;

Figure 7A is a graph of a filter response of a stop band pass filter;

Figure 7B is a graph of testing a stop band pass filter in accordance with the present invention;

Figure 8 is a schematic block diagram of a calibration configuration for a receiver section of a radio in accordance with the present invention;

Figure 9 is a logic diagram of a method for calibrating a filter in accordance with the present invention; and

Figure 10 is a logic diagram of a method for calibrating a low pass filter in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a schematic block diagram illustrating a communication system 10 that includes a plurality of base stations and/or access points 12-16, a plurality of wireless communication devices 18-32 and a network hardware component 34. The wireless communication devices 18-32 may be laptop host computers 18 and 26, personal digital assistant hosts 20 and 30, personal computer hosts 24 and 32 and/or cellular telephone hosts 22 and 28. The details of the wireless communication devices will be described in greater detail with reference to Figure 2.

The base stations or access points 12-16 are operably coupled to the network hardware 34 via local area network connections 36, 38 and 40. The network hardware 34, which may be a router, switch, bridge, modem, system controller, et cetera provides a

wide area network connection 42 for the communication system 10. Each of the base stations or access points 12-16 has an associated antenna or antenna array to communicate with the wireless communication devices in its area. Typically, the wireless communication devices register with a particular base station or access point 12-14 to receive services from the communication system 10. For direct connections (i.e., point-to-point communications), wireless communication devices communicate directly via an allocated channel.

Typically, base stations are used for cellular telephone systems and like-type systems, while access points are used for in-home or in-building wireless networks. Regardless of the particular type of communication system, each wireless communication device includes a built-in radio and/or is coupled to a radio. The radio includes a highly linear amplifier and/or programmable multi-stage amplifier as disclosed herein to enhance performance, reduce costs, reduce size, and/or enhance broadband applications.

Figure 2 is a schematic block diagram illustrating a wireless communication device that includes the host device 18-32 and an associated radio 60. For cellular telephone hosts, the radio 60 is a built-in component. For personal digital assistants hosts, laptop hosts, and/or personal computer hosts, the radio 60 may be built-in or an externally coupled component.

As illustrated, the host device 18-32 includes a processing module 50, memory 52, radio interface 54, input interface 58 and output interface 56. The processing module 50 and memory 52 execute the corresponding instructions that are typically done by the host device. For example, for a cellular telephone host device, the processing module 50 performs the corresponding communication functions in accordance with a particular cellular telephone standard.

The radio interface 54 allows data to be received from and sent to the radio 60. For data received from the radio 60 (e.g., inbound data), the radio interface 54 provides the data to the processing module 50 for further processing and/or routing to the output

interface 56. The output interface 56 provides connectivity to an output display device such as a display, monitor, speakers, et cetera such that the received data may be displayed. The radio interface 54 also provides data from the processing module 50 to the radio 60. The processing module 50 may receive the outbound data from an input device such as a keyboard, keypad, microphone, et cetera via the input interface 58 or generate the data itself. For data received via the input interface 58, the processing module 50 may perform a corresponding host function on the data and/or route it to the radio 60 via the radio interface 54.

Radio 60 includes a host interface 62, digital receiver processing module 64, an analog-to-digital converter 66, a filtering/gain module 68, an IF mixing down conversion stage 70, a receiver filter 71, a low noise amplifier 72, a transmitter/receiver switch 73, a local oscillation module 74, memory 75, a digital transmitter processing module 76, a digital-to-analog converter 78, a filtering/gain module 80, an IF mixing up conversion stage 82, a power amplifier 84, a transmitter filter module 85, and an antenna 86. The antenna 86 may be a single antenna that is shared by the transmit and receive paths as regulated by the Tx/Rx switch 73, or may include separate antennas for the transmit path and receive path. The antenna implementation will depend on the particular standard to which the wireless communication device is compliant. The filtering/gain modules 68 and/or 80 may include calibration circuitry as will be described with reference to Figures 3 - 10.

The digital receiver processing module 64 and the digital transmitter processing module 76, in combination with operational instructions stored in memory 75, execute digital receiver functions and digital transmitter functions, respectively. The digital receiver functions include, but are not limited to, digital intermediate frequency to baseband conversion, demodulation, constellation demapping, decoding, and/or descrambling. The digital transmitter functions include, but are not limited to, scrambling, encoding, constellation mapping, modulation, and/or digital baseband to IF conversion. The digital receiver and transmitter processing modules 64 and 76 may be implemented using a shared processing device, individual processing devices, or a

plurality of processing devices. Such a processing device may be a microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions. The memory 75 may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static memory, dynamic memory, flash memory, and/or any device that stores digital information. Note that when the processing module 64 and/or 76 implements one or more of its functions via a state machine, analog circuitry, digital circuitry, and/or logic circuitry, the memory storing the corresponding operational instructions is embedded with the circuitry comprising the state machine, analog circuitry, digital circuitry, and/or logic circuitry.

In operation, the radio 60 receives outbound data 94 from the host device via the host interface 62. The host interface 62 routes the outbound data 94 to the digital transmitter processing module 76, which processes the outbound data 94 in accordance with a particular wireless communication standard (e.g., IEEE 802.11 Bluetooth, et cetera) to produce digital transmission formatted data 96. The digital transmission formatted data 96 will be a digital base-band signal or a digital low IF signal, where the low IF typically will be in the frequency range of one hundred kilohertz to a few megahertz.

The digital-to-analog converter 78 converts the digital transmission formatted data 96 from the digital domain to the analog domain. The filtering/gain module 80 filters and/or adjusts the gain of the analog signal prior to providing it to the IF mixing stage 82. The IF mixing stage 82 converts the analog baseband or low IF signal into an RF signal based on a transmitter local oscillation 83 provided by local oscillation module 74. The power amplifier 84 amplifies the RF signal to produce outbound RF signal 98, which is filtered by the transmitter filter module 85. The antenna 86 transmits the

outbound RF signal 98 to a targeted device such as a base station, an access point and/or another wireless communication device.

The radio 60 also receives an inbound RF signal 88 via the antenna 86, which was transmitted by a base station, an access point, or another wireless communication device. The antenna 86 provides the inbound RF signal 88 to the receiver filter module 71 via the Tx/Rx switch 73, where the Rx filter 71 bandpass filters the inbound RF signal 88. The Rx filter 71 provides the filtered RF signal to low noise amplifier 72, which amplifies the signal 88 to produce an amplified inbound RF signal. The low noise amplifier 72 provides the amplified inbound RF signal to the IF mixing module 70, which directly converts the amplified inbound RF signal into an inbound low IF signal or baseband signal based on a receiver local oscillation 81 provided by local oscillation module 74. The down conversion module 70 provides the inbound low IF signal or baseband signal to the filtering/gain module 68. The filtering/gain module 68 filters and/or gains the inbound low IF signal or the inbound baseband signal to produce a filtered inbound signal.

The analog-to-digital converter 66 converts the filtered inbound signal from the analog domain to the digital domain to produce digital reception formatted data 90. The digital receiver processing module 64 decodes, descrambles, demaps, and/or demodulates the digital reception formatted data 90 to recapture inbound data 92 in accordance with the particular wireless communication standard being implemented by radio 60. The host interface 62 provides the recaptured inbound data 92 to the host device 18-32 via the radio interface 54.

As one of average skill in the art will appreciate, the wireless communication device of figure 2 may be implemented using one or more integrated circuits. For example, the host device may be implemented on one integrated circuit, the digital receiver processing module 64, the digital transmitter processing module 76 and memory 75 may be implemented on a second integrated circuit, and the remaining components of the radio 60, less the antenna 86, may be implemented on a third integrated circuit. As an

alternate example, the radio 60 may be implemented on a single integrated circuit. As yet another example, the processing module 50 of the host device and the digital receiver and transmitter processing modules 64 and 76 may be a common processing device implemented on a single integrated circuit. Further, the memory 52 and memory 75 may be implemented on a single integrated circuit and/or on the same integrated circuit as the common processing modules of processing module 50 and the digital receiver and transmitter processing module 64 and 76.

Figure 3 is a schematic block diagram of a filtering module 68 and/or 80 that includes a filtering circuit 100 and a calibration module 102. The filtering circuit 100, which may be a low pass filter, a bandpass filter, a stop band filter, or a high pass filter, includes a first adjustable filter element 108 and a second adjustable filter element 110. The particular types of components of the first and second adjustable filter elements 108 and 110 depend on the type of filtering desired. For example, for a low pass filter, the first adjustable filter element 108 may be an adjustable resistor and the second adjustable filter element 110 may be an adjustable capacitor.

The calibration module 102 includes a signal strength module 112, a comparator 114, and a response adjust module 116. In operation, a tone signal (i.e., a signal having a single frequency component) having a frequency well within the pass region of the filtering circuit 100 is provided to the input of the filtering circuit 100 as a received signal 104. Since this tone signal is well within the pass region of the filter, the filtered output signal 106 should substantially match the inputted tone signal. The signal strength module 112, which may be a received signal strength indicator, measures the signal strength of the filtered signal 106 of the first tone signal. This signal strength value is stored within the signal strength module 112. Next, a second tone signal is inputted to the filtering circuit 100, where second tone signal has a frequency at a corner frequency of the filtering circuit 100.

For example, if the filtering circuit 100 implements a single pole low pass filter, the corner frequency corresponds to the -3 dB point (i.e., the frequency at which a signal

is attenuated by approximately 1/3rd by the filter with respect to an unattenuated signal) as shown in Figure 4. While the desired corner frequency establishes the pass region (i.e., signals having frequencies in this region are passed substantially unattenuated) and the attenuation region (i.e., signals having frequencies in this region are attenuated based on the response of the filter). Due to limitations of the CMOS technology, a low pass filter will most likely not have the desired corner frequency, but one that is up to forty percent from the desired corner frequency, as illustrated by the shaded area.

Continuing with the low pass filter example, and with reference to Figure 5, the first filtered tone signal 124 has a frequency well within the pass region, thus its amplitude substantially matches the amplitude of the inputted tone signal. In one embodiment, to ensure that the first filtered tone signal 124 is within the pass region, the components of the filter are set to provide a maximum pass band. The second filtered tone signal 126 has a frequency at the desired corner frequency. The signal strength module 112 stores both signal strengths and compares them to establish an actual attenuation 118.

Returning to the discussion of Figure 3, the comparator compares the actual attenuation 118 is compared with the desired attenuation 120, which for a low pas filter is - 3 dB (i.e., the magnitude of the second filtered tone signal 126 should be approximately 2/3rds of the magnitude of the first filtered tone signal 124). If the actual attenuation 118 substantially matches the desired attenuation 120, the corner frequency of the low pass filter is at the desired frequency. If, however, the actual attenuation 118 is greater than the desired attenuation (i.e., the magnitude of the second filtered tone signal 126 is less than the desired 2/3rds the amplitude of the first filtered tone signal 124), the corner frequency is too low. In this instance, the response adjust module 116 generates an adjust filter response 122 that increases the value of the first and/or second adjustable filter element 108 and 110. Once the adjustment is made, the process is repeated until the actual attenuation 118 substantially matches the desired attenuation 120.

If the actual attenuation 118 is less than the desired attenuation 120 (i.e., the magnitude of the second filtered tone signal 126 is greater than the desired 2/3rds the amplitude of the first filtered tone signal 124), the corner frequency is too high. In this instance, the response adjust module 116 generates an adjust filter response 122 that decreases the value of the first and/or second adjustable filter element 108 and 110. Once the adjustment is made, the process is repeated until the actual attenuation 118 substantially matches the desired attenuation 120. As such, the value of one or both of the adjustable filter elements 108 and 110 may be incrementally adjusted to achieve the desired attenuation, i.e., the desired corner frequency. Alternatively, the response adjust module 116 may determine the amount of difference between the actual attenuation 118 and the desired attenuation 120. Based on the difference, the response adjust module 116 determines the adjust filter response 122.

The calibration filter of Figure 3 may be a low pass filter, as described with reference to Figure 4, a high pass filter, a bandpass filter, or a stop band filter. Figures 5A and 5B illustrate the calibration of a high pass filter. Figure 5A illustrates the frequency response of a single pole, or first order, high pass filter that includes an attenuation region and a pass region. The desired corner frequency delineates these two regions. The calibration of the high pass filter is shown in Figure 5B. The calibration begins by providing a first tone signal that has a frequency well within the pass region. The filtered first tone signal 124 is shown to have a first magnitude, or signal strength. The calibration continues by providing a second tone signal that has a frequency at the desired corner frequency of the high pass filter. The filtered second tone signal 126 is shown to have a second magnitude, or signal strength, that is less than that of the filtered first tone signal 124. The actual attenuation 118 is determined based on the difference signal strength of the first and second filtered tone signals 124 and 126, which is subsequently compared to the desired attenuation. Based on this comparison, the components of the high pass filter are adjusted to obtain the desired corner frequency.

Figures 6A and 6B illustrate the calibration of a bandpass filter. Figure 6A illustrates the frequency response of a first order bandpass filter that includes two

attenuation regions and a pass region. The desired corner frequencies delineate the pass region from the two attenuation regions. The calibration of the bandpass filter is shown in Figure 6B. The calibration begins by providing a first tone signal that has a frequency well within the pass region. The filtered first tone signal 124 is shown to have a first magnitude, or signal strength. The calibration continues by providing a second tone signal that has a frequency at one of the desired corner frequencies of the bandpass filter. The filtered second tone signal 126 is shown to have a second magnitude, or signal strength, that is less than that of the filtered first tone signal 124. The actual attenuation 118 for this corner frequency is determined based on the difference signal strength of the first and second filtered tone signals 124 and 126, which is subsequently compared to the desired attenuation. Based on this comparison, the components of the bandpass filter are adjusted to obtain the desired corner frequency for this corner frequency. The calibration further includes providing a third tone signal that has a frequency at the other desired corner frequency of the bandpass filter. The filtered third tone signal 128 is shown to have a third magnitude, or signal strength, that is less than that of the filtered first tone signal 124. The actual attenuation 118 for this corner frequency is determined based on the difference signal strength of the first and third filtered tone signals 124 and 128, which is subsequently compared to the desired attenuation. Based on this comparison, the components of the bandpass filter are adjusted to obtain the desired corner frequency for this corner frequency.

Figures 7A and 7B illustrate the calibration of a stop band filter. Figure 7A illustrates the frequency response of a first order stop band filter that includes two pass regions and an attenuation region. The desired corner frequencies delineate the attenuation region from the two pass regions. The calibration of the stop band filter is shown in Figure 7B. The calibration begins by providing a first tone signal that has a frequency well within the first pass region or the second pass region. The filtered first tone signal 124 is shown to have a first magnitude, or signal strength. The calibration continues by providing a second tone signal that has a frequency at one of the desired corner frequencies of the stop band filter. The filtered second tone signal 126 is shown to have a second magnitude, or signal strength, that is less than that of the filtered first tone

signal 124. The actual attenuation 118 for this corner frequency is determined based on the difference signal strength of the first and second filtered tone signals 124 and 126, which is subsequently compared to the desired attenuation. Based on this comparison, the components of the stop band filter are adjusted to obtain the desired corner frequency for this corner frequency. The calibration further includes providing a third tone signal that has a frequency at the other desired corner frequency of the stop band filter. The filtered third tone signal 128 is shown to have a third magnitude, or signal strength, that is less than that of the filtered first tone signal 124. The actual attenuation 118 for this corner frequency is determined based on the difference signal strength of the first and third filtered tone signals 124 and 128, which is subsequently compared to the desired attenuation. Based on this comparison, the components of the stop band filter are adjusted to obtain the desired corner frequency for this corner frequency.

Figure 8 is a schematic block diagram of a calibration configuration for the low pass filters (LPF) 86 of a radio receiver. In this configuration, the output of a power amplifier 84 is coupled to the input of the low noise amplifier 72. Thus, test signals (i.e., the tone signals) may be inputted to the mixers of the up conversion module 82. The mixers mix the test signals with a local oscillation to produce RF signals. The RF signals are received by the low noise amplifier 72 and provided to the mixers of the down conversion module 70. The mixers of the down conversion module 70 mix the received RF signals with a local oscillation to produce base band, or low intermediate frequency, signals that include an in-phase component [I(t)] and a quadrature component [Q(t)]. The low pass filters 86-1 and 86-2 filter the in-phase component and the quadrature component, respectively.

In this embodiment, the signal strength module 112 includes two integrators 140 and 142, a summation module 145, two registers 146 and 148, and a subtraction module 147. The integrators 140 and 142 integrate the absolute values of the filtered I and Q components to obtain a corresponding energy of the two components. The summation module 145 adds the energy components together to obtain the measured signal strength 144. If the signal being processed corresponds to the first tone signal (i.e., the signal

having a frequency well within the pass region of the filter), the measured signal strength 144 is stored in the first signal strength register 146. If, however, the signal corresponds to the second tone signal (i.e., the signal having a frequency at the desired corner frequency), the measured signal strength is stored in the second signal strength register 148. Once the signal strengths of the first and second tone signals have been stored, the subtraction module 147 subtracts the measured signal strength of the second tone signal from the measured signal strength of the first tone signal to produce the actual attenuation 118.

The comparator 114 compares the actual attenuation 118 with the desired attenuation 120 to produce an indication of the filter response. The response adjust module 116 interprets the output of the comparator 114 to generate the adjust filter response signal 122.

Figure 9 is a logic diagram of a method for calibrating a filter that begins at step 150 where a filter filters a first signal having a first frequency to produce a first filtered signal, wherein the first frequency is in a known pass region of the filter. The filter may be of various embodiments including a low pass filter, a bandpass filter, a high pass filter, and/or stop band filter. The processing continues at step 152 where the signal strength of the first filtered signal is measured to produce a first measured signal strength. The processing continues at step 154 where the filter filters a second signal having a second frequency to produce a second filtered signal, wherein the second frequency is at a desired corner frequency of the filter. The processing continues at step 156 where the signal strength of the second filtered signal is measured to produce a second measured signal strength.

The processing continues at step 158 where the first measured signal strength is compared with the second measured signal strength to determine whether the filter has attenuated the second signal by a desired attenuation value with respect to the first signal. If yes, the process proceeds to step 164 where the desired filter response is obtained. If not, the process proceeds to step 162 wherein the filter response of the filter is adjusted to

produce an adjusted filter response. Once the filter response has been adjusted, the process may repeat at step 150 if the adjustment is based on an incremental adjustment process.

Figure 10 is a logic diagram of a method for calibrating a receiver low pass filter that begins at step 170 where the filter response of the receiver low pass filter is set to an initial state (e.g., to have the highest corner frequency possible or the lowest corner frequency possible based on adjustability of the low pass filter components). The processing continues at step 172 where the receiver low pass filter filters a first signal having a first frequency to produce a first filtered signal, wherein the first frequency is in a known pass region of the filter. The process continues at step 174 where the signal strength of the first filtered signal is measured to produce a first measured signal strength. The processing then continues at step 174 where the receiver low pass filter filters a second signal having a second frequency to produce a second filtered signal, wherein the second frequency is at a desired corner frequency of the filter. The processing continues at step 178 where the signal strength of the second filtered signal is measured to produce a second measured signal strength.

The process continues at step 180 where the first measured signal strength is compared with the second measured signal strength to determine whether the filter has attenuated the second signal by a desired attenuation value with respect to the first signal. If yes, the process proceeds to step 184 where the desired filter response is obtained. If not, the process proceeds to step 186 where the filter response of the receiver low pass filter is adjusted to produce an adjusted filter response. The process may then continue at step 172 with the new settings for the low pass filter.

As one of average skill in the art will appreciate, the term "substantially" or "approximately", as may be used herein, provides an industry-accepted tolerance to its corresponding term. Such an industry-accepted tolerance ranges from less than one percent to twenty percent and corresponds to, but is not limited to, component values,

integrated circuit process variations, temperature variations, rise and fall times, and/or thermal noise. As one of average skill in the art will further appreciate, the term "operably coupled", as may be used herein, includes direct coupling and indirect coupling via another component, element, circuit, or module where, for indirect coupling, the intervening component, element, circuit, or module does not modify the information of a signal but may adjust its current level, voltage level, and/or power level. As one of average skill in the art will also appreciate, inferred coupling (i.e., where one element is coupled to another element by inference) includes direct and indirect coupling between two elements in the same manner as "operably coupled". As one of average skill in the art will further appreciate, the term "compares favorably", as may be used herein, indicates that a comparison between two or more elements, items, signals, etc., provides a desired relationship. For example, when the desired relationship is that signal 1 has a greater magnitude than signal 2, a favorable comparison may be achieved when the magnitude of signal 1 is greater than that of signal 2 or when the magnitude of signal 2 is less than that of signal 1.

The preceding discussion has presented a method and apparatus for accurate calibration of on chip filters. As one of average skill in the art will appreciate, the concepts of the present invention work for higher order filters than the ones presented in Figures 3 - 10. As one of average skill in the art will further appreciate, other embodiments may be derived from the teachings of the present invention without deviating from the scope of the claims.